REMARKS/ARGUMENTS

Brief Summary of Status

Claims 1-30 are pending in the application.

Claims 1-7 and 16-30 are allowed.

Claim 8 is rejected.

Claims 8-15 are objected to.

35 U.S.C. § 112

4. The Examiner asserts:

"Claims 8 to 15 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The components that perform the decoding function critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See In re Mayhew, 527 F.2d 1229,188 USPQ 356 (CCPA 1976). The disclosure describes low density parity check decoding process with respect to figures (19 to 22) wherein the decoder includes edge messages, a bit node calculator, and a check node calculator for performing decoding of a low density parity check (LDPC) code." (office action, Part of Paper No./Mail Date 20060201, p. 2)

6. The Examiner asserts:

"Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the edge messages, the bit node calculator and the check node calculator necessary for the decoder to perform its decoding function as defined in the specification. Claims 9 to 15 are also rejected due to their dependency on a rejected base claim." (office action, Part of Paper No./Mail Date 20060201, p. 3)

35 U.S.C. § 102

8. The Examiner asserts:

"Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Coker et al. (USPAP 2003/0074626 A1)." (hereinafter referred to as "Coker") (office action, Part of Paper No./Mail Date 20060201, p. 3)

Allowable Subject Matter

9. The Examiner asserts:

"Claims 8 to 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." (office action, Part of Paper No./Mail Date 20060201, p. 6)

35 U.S.C. § 112

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"Claims 8 to 15 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The components that perform the decoding function critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See In re Mayhew, 527 F.2d 1229,188 USPQ 356 (CCPA 1976). The disclosure describes low density parity check decoding process with respect to figures (19 to 22) wherein the decoder includes edge messages, a bit node calculator, and a check node calculator for performing decoding of a low density parity check (LDPC) code." (office action, Part of Paper No./Mail Date 20060201, p. 2)

The Applicant has amended claims 8 to include subject matter that includes at least a check node update functional block, a symbol sequence estimate and symbol node update functional block, and a plurality of edge messages that corresponds to a plurality of edges that communicatively couple a plurality of symbol nodes to a plurality of check nodes within an LDPC (Low Density Parity Check) coded modulation bipartite graph that corresponds to an LDPC code.

Given the amendment to claim 8, the Applicant respectfully believes that the rejections of claims 9-15 under 35 U.S.C. § 112, first paragraph, have also been addressed given that claims 9-15 are further limitations of the subject matter as claimed in independent claim 8.

As such, the Applicant respectfully requests that the Examiner withdraw the rejections of claims 8-15 under 35 U.S.C. § 112, first paragraph.

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"Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the edge messages, the bit node calculator and the check node calculator necessary for the decoder to perform its decoding function as defined in the specification. Claims 9 to 15 are also rejected due to their dependency on a rejected base claim." (office action, Part of Paper No./Mail Date 20060201, p. 3)

The Applicant has amended claims 8 to include subject matter that includes at least a check node update functional block, a symbol sequence estimate and symbol node update functional block, and a plurality of edge messages that corresponds to a plurality of edges that communicatively couple a plurality of symbol nodes to a plurality of check nodes within an LDPC (Low Density Parity Check) coded modulation bipartite graph that corresponds to an LDPC code.

As such, the Applicant respectfully requests that the Examiner withdraw the rejections of claim 8 under 35 U.S.C. § 112, second paragraph.

35 U.S.C. § 102

8. The Examiner asserts:

"Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Coker et al. (USPAP 2003/0074626 A1)." (hereinafter referred to as "Coker") (office action, Part of Paper No./Mail Date 20060201, p. 3)

The Applicant respectfully traverses.

The Applicant has amended certain of the claims.

The Applicant respectfully points out that, in order to support a proper rejection under 35 U.S.C. §102, a singular reference must teach and disclose each and every limitation of the subject matter as claimed by the Applicant. If the singular reference fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant, the rejections under 35 U.S.C. § 102 are improper and should be withdrawn.

The Applicant respectfully points out that Coker fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant.

With respect to claim 8, the Examiner also asserts:

"Coker teaches the claimed invention of a method for decoding low density parity check (LDPC) codes using a multi-level decoder (140) that receives multi-level symbols (see par. 0028)." (office action, Part of Paper No./Mail Date 20060201, p. 3)

The Applicant respectfully points out that the edges of Coker do not communicatively couple between actual "symbol nodes" and "check nodes" at all.

In contradistinction, the edges of Coker actually connect between nodes that actually correspond to individual "bits" of code word and "check nodes". The use of terminology of Coker is somewhat ambiguous/unclear, and the Applicant understands where possible confusion could arise with reference to the "symbol nodes" of Coker, which actually seem to correspond to "bits" (i.e., and not an entire symbol).

Coker teaches and discloses:

"The SPA operates on a bipartite graph associated with a given sparse parity check matrix H having M rows and N columns. This graph has two types of nodes: N symbol nodes corresponding to each bit in a code word x, and M check nodes corresponding to the parity checks $pc_m(x)$, $1 \leq m \leq M$, represented by the rows of the matrix H. Each symbol node is connected to the check nodes it participates in, and each check node is connected to the symbol nodes it checks. The SPA operates by passing messages between symbol nodes and check nodes. The messages themselves can be a posterioiri probabilities (APP) or log likelihood ratios (LLRs). Typical message parsing schedules alternately compute updates of all symbol nodes and of all check nodes." (Coker, paragraph 0045, lines 6-end of paragraph, emphasis added)

Coker explicitly teaches and discloses that the bipartite graph employed therein has two types of nodes, "symbol nodes" and "check nodes", and specifically the "symbol nodes corresponding to each bit in a code word x". In other words, these "symbol nodes" of Coker do not correspond to more than 1 bit.

Coker explicitly teaches and discloses that the "symbol nodes" correspond to "each bit in a code word". In other words, these "symbol nodes" of Coker are actually "bit nodes", which is the common term typically employed in the art for such nodes wherein each such node of the LDPC bipartite graph corresponds to one bit.

Furthermore, Coker explicitly teaches and discloses that the "SPA operates by passing messages between symbol nodes and check nodes", and since each of the "symbol nodes" of Coker corresponds to only one "bit in a code word". then these "messages" of Coker cannot correspond to edges that communicatively couple actual "symbol nodes" (as disclosed and claimed by the Applicant) and "check nodes".

The Applicant teaches and discloses the distinction between symbol nodes, bit nodes, and check nodes. In at least FIG. 24A, FIG. 24B, and the corresponding written

specification portions of the Applicant's originally filed disclosure, the Applicant shows the distinction between bit nodes, symbol nodes, and check nodes. FIG. 24B of the Applicant's originally filed disclosure shows how the symbol nodes can be directly connected to the check nodes in accordance with certain aspects of the Applicant's invention when performing the appropriate novel labeling of the Applicant.

In one such possible embodiment, the edge messages of the FIG. 24B correspond to the edges that communicatively couple the symbol nodes and the check nodes of the LDPC coded modulation bipartite graph. It can be seen that an actual "symbol node" (as disclosed and claimed by the Applicant) actually corresponds to more than one bit.

In contradistinction, Coker explicitly teaches and discloses the "symbol nodes corresponding to each bit in a code word x". In other words, each of these "symbol nodes" of Coker actually corresponds to only one bit.

Although Coker employs the use of the terminology of "symbol nodes", Coker explicitly teaches and discloses that these "symbol nodes" correspond to the individual bits of the LDPC codeword. In addition to the portion of Coker cited above that points out this relationship (i.e., of "symbol nodes" corresponding to "each bit in a code word), the Applicant cites the following portions of Coker that also explicitly depict this relationship within Coker.

Coker teaches and discloses:

"A method for decoding Low Density Parity Check (LDPC) codes comprises executing a sum product algorithm to recover a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes, the sum product algorithm being responsive to input log likelihood ratios associated with the symbol nodes." (Coker, ABSTRACT, lines 1-6, emphasis added)

"... a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes ..." (Coker, claims 1, 4, 6, and 8)

"... a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes ..." (Coker, SUMMARY OF THE INVENTION, paragraph 0010)

"... a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes ..." (Coker, paragraph 0084)

It seems clear to the Applicant that the LDPC bipartite graph corresponds to "a set of information bits from an LDPC code" and not to symbols "from an LDPC code".

It seems clear to the Applicant that the LDPC bipartite graph employed by Coker includes "check nodes" and what should more properly be referred to as "bit nodes" (although Coker refers to them as "symbol nodes").

Throughout Coker, Coker indicates that "a set of information bits", and not the symbols therein, is represented by "an LDPC code represented as a bipartite graph of symbol nodes and check nodes".

This, coupled with the fact that Coker explicitly teaches and discloses the "symbol nodes corresponding to each bit in a code word x", leads the Applicant to the understanding that the "symbol nodes" of Coker are actually what are typically referred to in the art as "bit nodes".

Furthermore, in contradistinction to the disclosure of the Applicant which provides detail regarding the distinction between symbol nodes, bit nodes, and check nodes, Coker provides no such clarification and distinction whatsoever.

In fact, Coker does not disclose even once the term "bit node", yet Coker explicitly teaches and discloses that the "symbol nodes" referred to therein are the "symbol nodes corresponding to each bit in a code word x".

Coker seems consistent in his mis-labeling of his "symbol nodes" with what are typically referred to in the art as "bit nodes", in that, everywhere where it would seem appropriate to employ the term "bit node" within Coker, Coker employs the term "symbol node". Again, Coker teaches and discloses that each "symbol node" of his corresponds to "each bit in a code word".

Moreover, it seems also clear to the Applicant that Coker does not intend his symbol nodes to correspond to more than one bit because (1) Coker explicitly teaches and discloses the "symbol nodes corresponding to each bit in a code word x" (i.e., a one to one relationship between symbols nodes and bits of the code word), and (2) Coker fails to teach and disclose any labeling or appropriate handling of messages connecting between the "symbol nodes" and the "check nodes" of Coker.

If Coker did intend to teach and disclose actual "symbol nodes" as the Applicant does, Coker would need to deal with the relationship between "bit nodes" and "symbol nodes". However, Coker does not do this.

When using actual "symbol nodes" as disclosed by the Applicant (in at least the Applicant's FIG. 24A and associated written description), it is clear that some edges correspond to more than 1 bit. Because of this, there has to be an appropriate handling of the correspondence between the multiple bits represented by a singular actual "symbol node" and the "bit nodes" to which the "symbol node" corresponds.

The Applicant teaches and discloses:

"With respect to the LDPC code bipartite graphs described above, it is noted that the labels of some of the edges correspond to more than 1 bit. For example, for the bits 3, 5, 6, and 7, the edge messages correspond to more than 2 values. Because of this, the common approach of employing LLR (log likelihood ratio) decoding cannot be employed." (Applicant's specification, p. 49, lines 1-3).

The Applicant respectfully points out that Coker explicitly teaches and discloses throughout his disclosure that the LLR decoding approach is a possible decoding approach. This alone leads the Applicant to the belief that Coker's "symbol nodes" are not in fact actual "symbol nodes" as disclosed and claimed by the Applicant.

When referring to the messages that are passed between the "symbol nodes" and the "check nodes" of Coker (i.e., "SPA operates by passing messages between symbol nodes and check nodes"), Coker teaches and discloses:

"The messages themselves can be a posteroiri probabilities (APP) or log likelihood ratios (LLRs)." (Coker, paragraph 0008 and paragraph 0045, emphasis added)

"In a preferred embodiment of the present invention, LLRs are employed as messages in place of APPs. This permits replacement of the multiplications in Step 2 of the SPA with additions. Step 3 can also be easily adapted for LLRs. Advantageously, LLRs can also be efficiently used in Step 1 without converting between LLRs and APPs." (Coker, paragraph 0062)

Even more so when considering Coker, the reduced "computational complexity" in decoding processing of Coker does not seem to be associated whatsoever with the use of a modified bipartite graph that includes edges that communicatively couple actual

"symbol nodes" and "check nodes". In contradistinction, Coker focuses on approximations that are performed in the check node update processing steps.

Coker teaches and discloses:

"In a preferred embodiment of the present invention, an approximate check node update is based on a difference-metric approach on a two state trellis. This approach employs a dual max. approximation. The aforementioned Fossorier reference describes an example of a dual max. approximation. The approach can be thought of as similar to a Viterbi algorithm on a two state parity check trellis. The approach uses the difference of state metrics, i.e., the difference of logs, which is the LLR of the probabilities. The approach is recursive and requires one sign bit manipulation and one comparison at a time. This greatly simplifies computational implementation and facilitates parallel recursive operation in a general purpose Digital Signal Processor (DSP) environment, or in an application specific integrated circuit (ASIC) or similar custom logic design.

In a particularly preferred embodiment of the present invention, the performance of the algorithm is improved by introduction of a correction factor. The correction factor involves the addition of a constant at every recursive step. The added constant can be viewed as a fixed offset with the appropriate polarity. The addition does not significantly increase computational complexity. It is found that the correction factor brings the performance of the algorithm to within 0.05 dB of the performance of the full SPA." (Coker, paragraphs 0047 and 0048, emphasis added)

The Applicant is unable to find within Coker any teaching and disclosure of any subject matter related to the relationships between bit nodes, symbol nodes, and check nodes.

Since the "symbol nodes" of Coker appear actually to be "bit nodes" (as pointed out in numerous locations and citations of Coker above), the Applicant respectfully believes that Coker fails to teach and disclose the limitations of the subject matter as claimed by the Applicant in claim 8.

Therefore, in light of at least these comments made above, the Applicant respectfully believes that Coker fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in independent claims 8.

As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claim 8 under 35 U.S.C. § 102(e) as being anticipated by Coker.

Allowable Subject Matter

9. The Examiner asserts:

"Claims 8 to 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." (office action, Part of Paper No./Mail Date 20060201, p. 6)

The Applicant respectfully believes that the Examiner means to indicate that "Claims 9 to 15 are objected to" in the above cited portion of the office action, as claim 8 is an independent claim. If this belief of the Applicant is incorrect, the Applicant respectfully requests clarification from the Examiner.

The Applicant respectfully believes that claims 9-15, being further limitations of the subject matter as claimed in independent claim 8, are also allowable.

As such, the Applicant respectfully requests that the Examiner withdraw the objections to claims 8-15.

The Applicant respectfully believes that claims 1-30 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present U.S. utility patent application.

RESPECTFULLY SUBMITTED,

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